



Company Overview

May 2010

Safe Harbor

This presentation and the accompanying speaker's remarks may contain forward-looking statements made in reliance on the Safe Harbor provisions of the Private Securities Litigation Reform Act of 1995. Forward-looking statements involve risks and uncertainties that could cause actual results to differ significantly from those projected.

Material factors that may cause results to differ from the statements made include delays, setbacks or losses relating to our intellectual property or intellectual property litigations, or any invalidation or limitation of our key patents; fluctuations in our operating results due to the timing of new license agreements and royalties, or due to legal costs; changes in patent laws, regulation or enforcement, or other factors that might affect our ability to protect our intellectual property; the risk of a decline in demand for semiconductor products; failure by the industry to adopt our technologies; competing technologies; the future expiration of our patents; the future expiration of our license agreements and the cessation of related royalty income; the failure or refusal of licensees to pay royalties; failure to achieve the growth prospects and synergies expected from acquisition transactions; and delays and challenges associated with integrating acquired companies with our existing businesses.

You are cautioned not to place undue reliance on the forward-looking statements, which speak only as of the date of this presentation. Tessera's filings with the Securities and Exchange Commission, including its Annual Report on Form 10-K for the year ended December 31, 2009, and its Quarterly Report on Form 10-Q for the quarter ended March 31, 2010, include more information about factors that could affect the company's financial results.

Tessera assumes no obligation to correct or update information contained in this presentation.



Develops and monetizes innovative **miniaturization** technologies, which are differentiated by intellectual property content, through licensing or product sales

Wireless



Computing



Consumer



Delivering What the Industry Needs Most

INNOVATION

Providing “Product Enabling” Solutions

Faster Time-to-Market, Higher Product Performance

INVESTMENT

Lowering Customer R&D Costs

Access to Industry-Leading Innovation

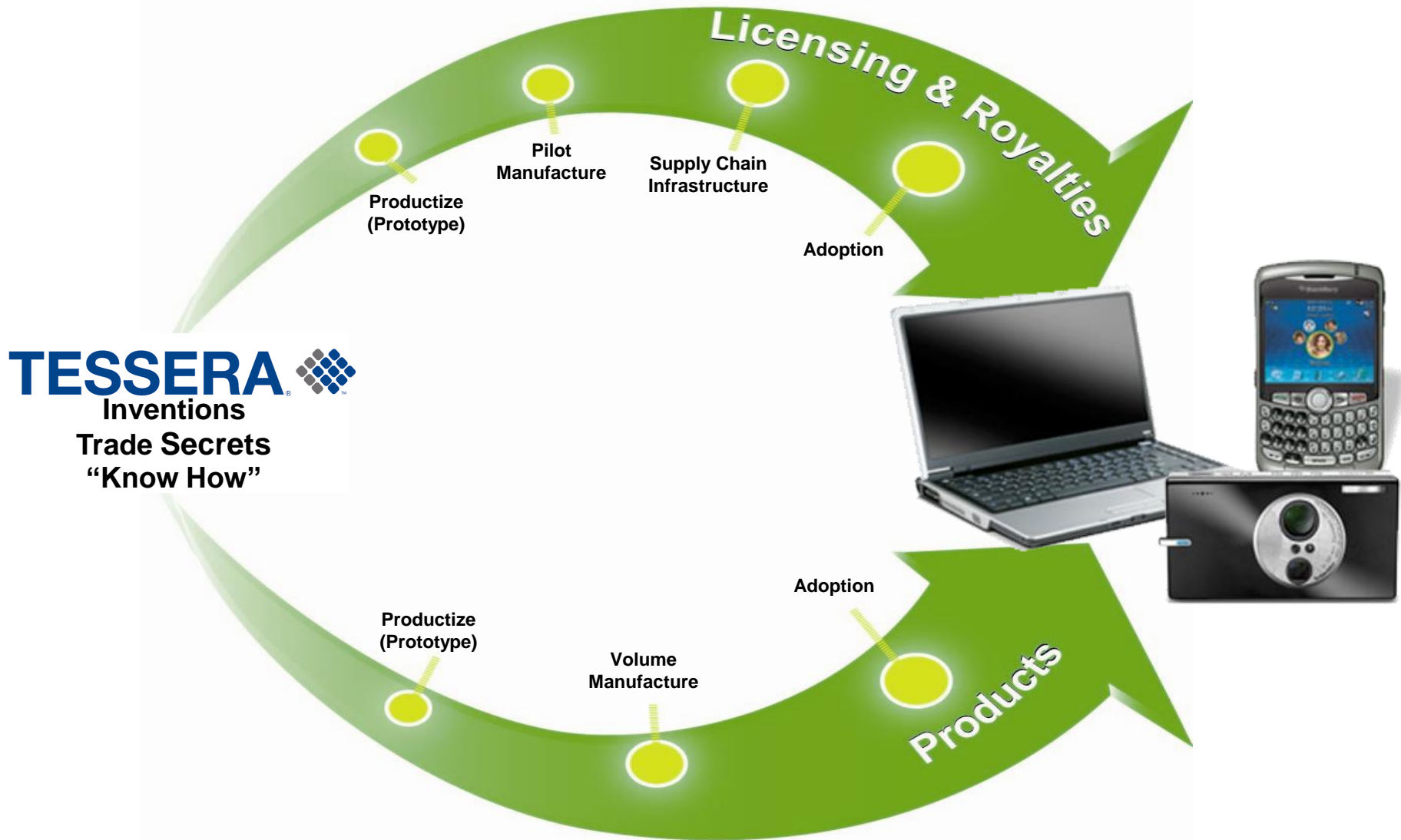
TESSERA 

INFRASTRUCTURE

Enabling Broad Adoption

System-Level Integration Across the Supply Chain

Developing and Driving Adoption



Select Current Licensees

Broad Use of Tessera Technologies



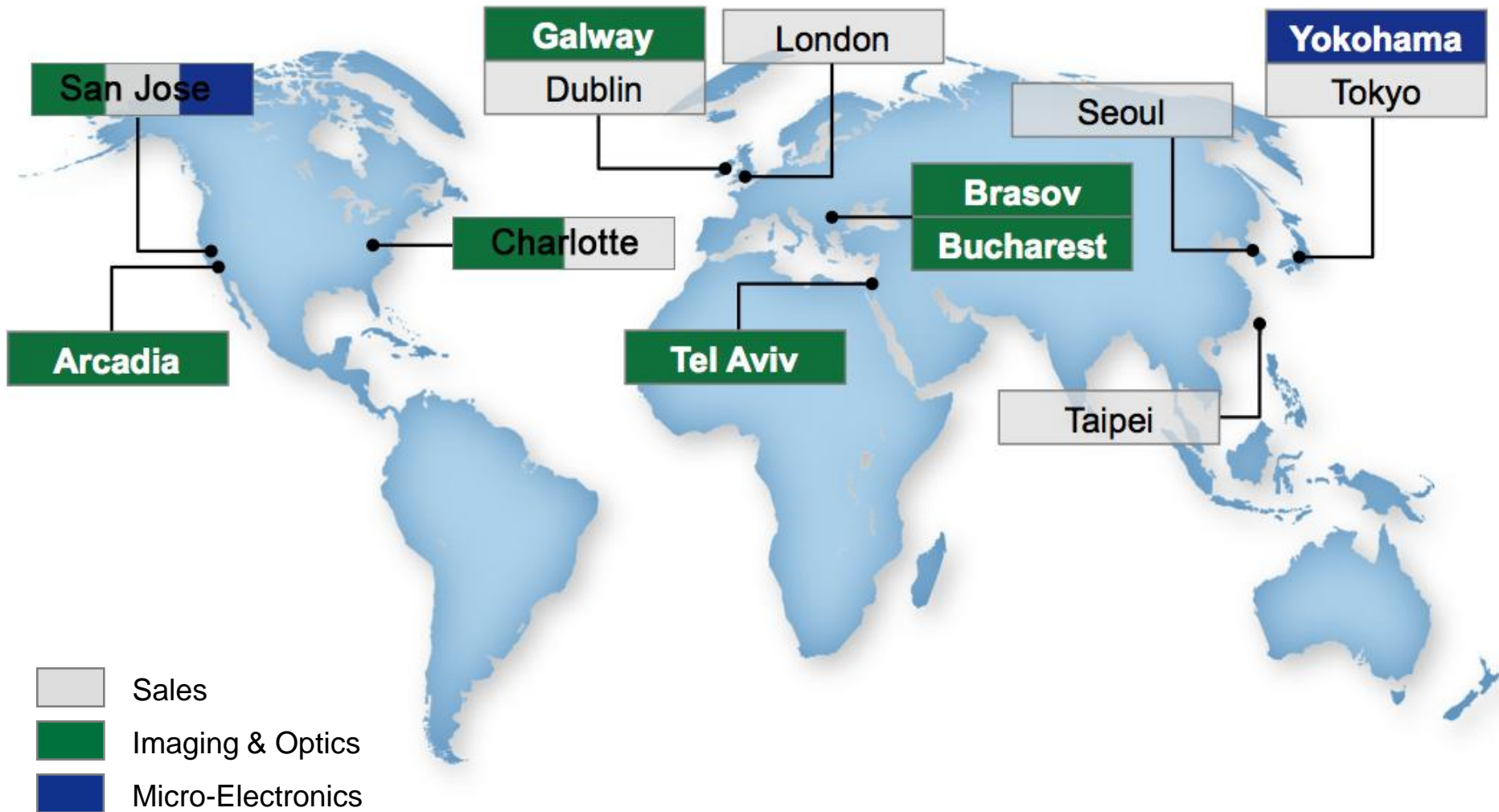
The Edison Labs of the 21st Century

Ongoing Investment in Innovation



- \$65.1 million R&D investment in TTM
- 299 dedicated technologists (63% of employees)
- 53 PhDs (11% of technologists)
- Global organization
- Robust patent portfolio – approximately 1,900 worldwide patent and patent applications at end of First Quarter 2010

Established Global Presence



TESSERA 

Micro-Electronics

Transforming Semiconductor Packaging

Packaging & Interconnect

Thermal Management

Wafer-Level Packaging

Imaging & Optics

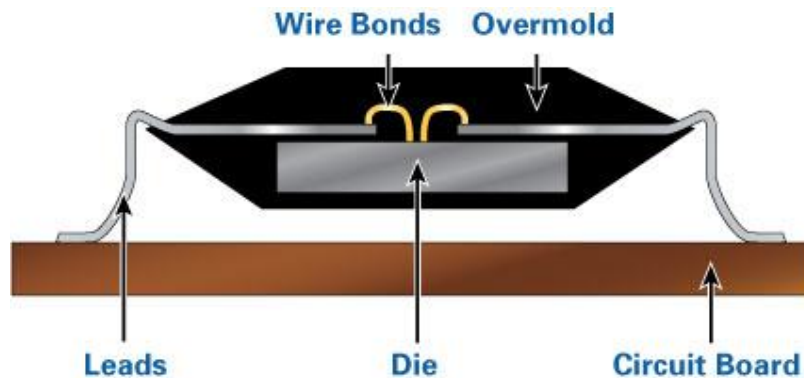
Transforming Image Capture & Processing

Image Enhancement

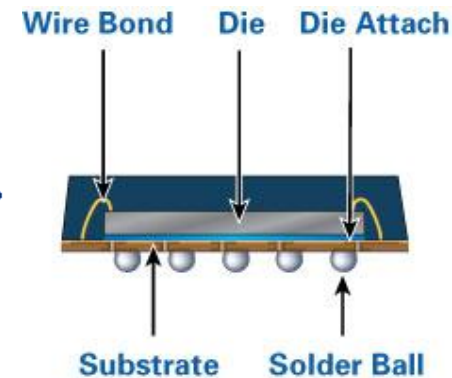
Wafer-Level Optics

Tessera CSP Revolutionizes Packaging

Thin Small Outline Package (TSOP)

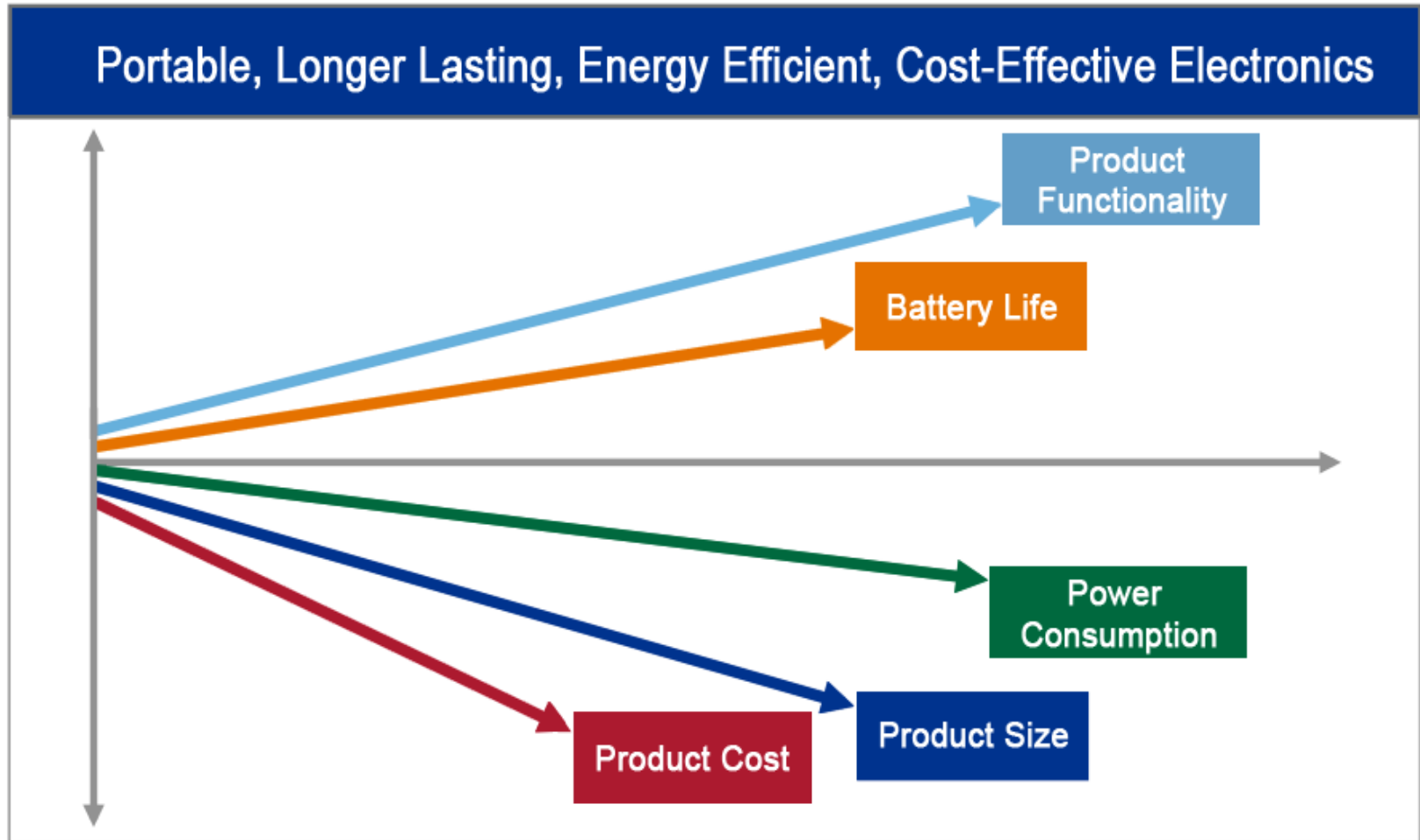


Chip Scale Package (CSP)

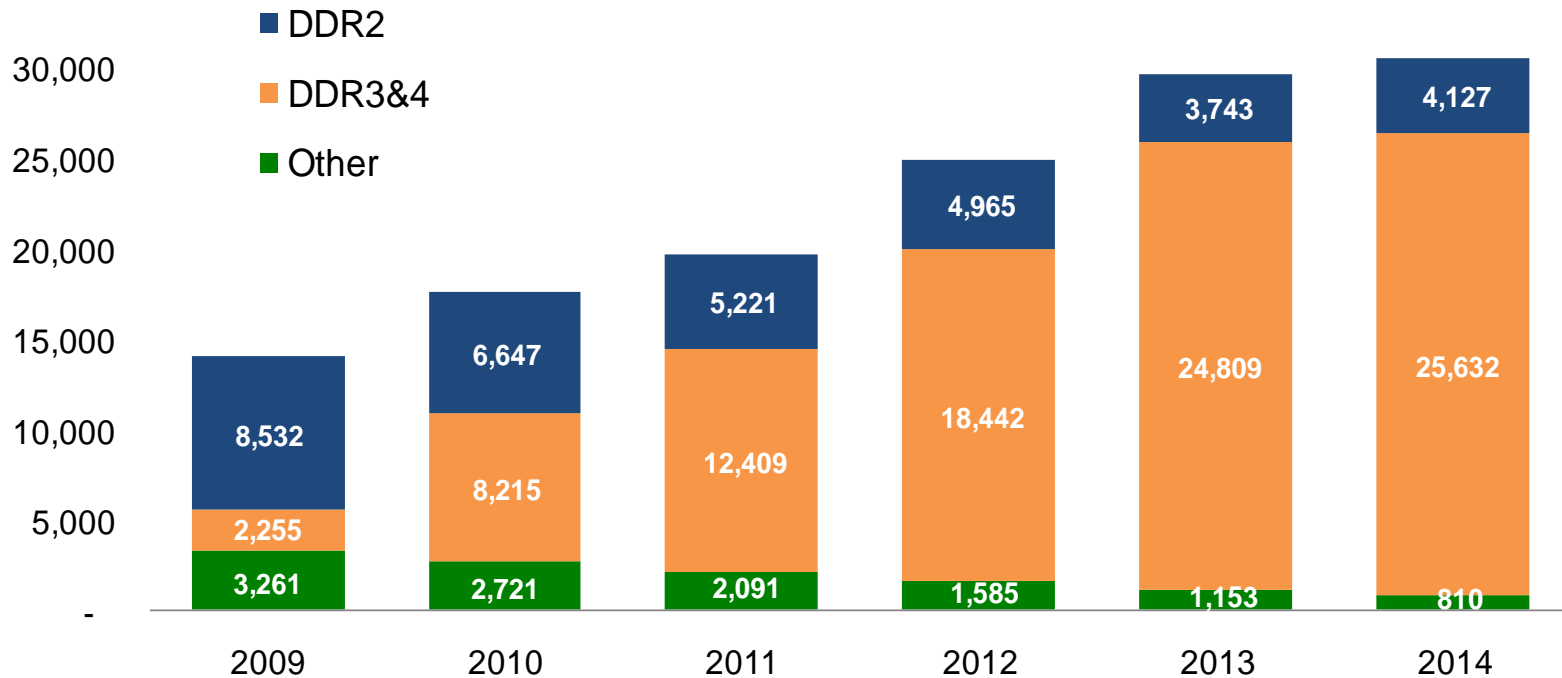


- Higher chip performance requirements create thermal cycling stress
- Tessera's CSP greatly improves reliability and enables significant reduction in form factor
- Industry invested heavily in CSP packaging

Opportunity: Price / Performance / Size Optimization



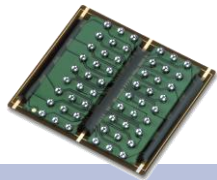
CSP for High-Performance Memory Today & Beyond



- DDR3 remains mainstream memory solution beyond 2013
 - Will be extended to higher frequencies (1600→1866 → 2133+ MHz) and lower voltages
 - DDR4 not defined; being pushed out further → possibly 2014
- Tessera CSP technology can meet DDR3+ performance & cost requirements today
- Additional Tessera patents, trade secrets and “know how” for DRAM CSP extend well beyond 2012

Source: Gartner, Feb. 2010

Tessera Packaging & Interconnect



Chip-Scale
Packaging

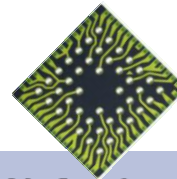
TCC® Technology

Technology for enabling
integrated, high-performance
electronic devices

- Smaller form factor (>80% area reduction)
- Higher performance (>200% inductance reduction)
- Higher reliability



**>50 Billion
Semiconductors
Shipped with Tessera IP**



Wafer-level
Packaging

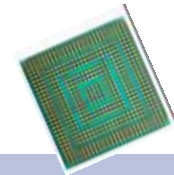
SHELLCASE® Technology

Technology for enabling
highly reliable, ultra-thin
electronic devices

- Ultra-thin “true die” profile (>40% height reduction)
- Robust interconnection (industry’s first TSV solution)
- Higher reliability



**>1 Billion
Image Sensors
Use Tessera IP**



Interconnect
Technologies

μPILR™ Platform

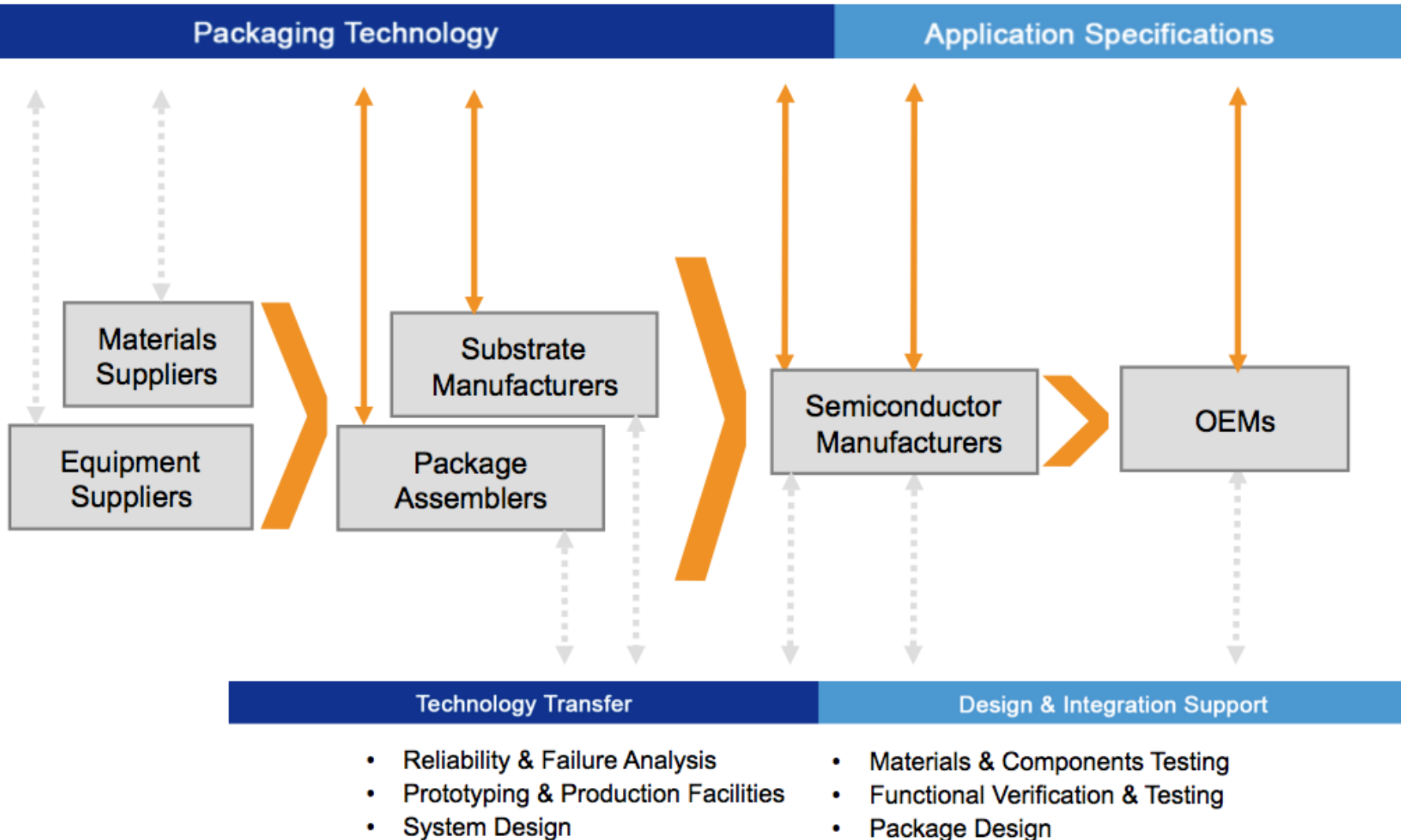
Technology for enabling
smaller, thinner, feature rich
electronic devices

- Finer pitch (>35% area reduction)
- Lower profile (>50% height reduction)
- Higher reliability



**Qualified
Substrate
Manufacturing**

Enabling the Supply Chain through Partnership



Next-Generation Innovation



Notebooks



Games



Projectors



Desktop Servers

**Thermal
Management**

Silent Air Cooling Technology

**Technology for enabling quieter, thinner,
more efficient devices**

- Silent: better user experience
- Reduced volume & mass: thinner, lighter
- Flexible form factor: choice of product design
- Improved cooling efficiency: longer battery life



**Ongoing Development
and Optimization**

TESSERA 

Micro-Electronics

Transforming Semiconductor Packaging

Packaging & Interconnect

Thermal Management

Wafer-Level Packaging

Imaging & Optics

Transforming Image Capture & Processing

Image Enhancement

Wafer-Level Optics

Transforming Image Capture & Processing

Image Capture and Video



Gaming



Bar Code Recognition



Augmented Reality



Gesture Control



Notebooks



Toys



Auto



Gaze



Security



Medical



“Smart Modules”
for Image Capture,
Process, Display
to Enable New
Apps and Usage

1 Billion+ Units Today
(< \$2 per VGA Camera)

Human Viewable

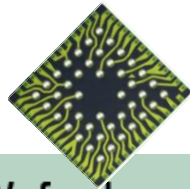


3+ Billion Units/yr within 5 Years

Machine Viewable

Imaging & Optics: Wafer-Level Innovation

Infrastructure
Technology



Wafer-Level
Packaging

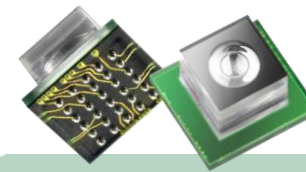
SHELLCASE® Technology

Technology for enabling smaller, thinner, low-cost image sensor devices

- Smaller footprint, true CSP (>35% area reduction)
- Lower cost
- Higher reliability
- Through-Silicon-Via technology



**>1 Billion Image Sensors
Use Tessera IP**



Wafer-Level
Optics

OptiML™ Technology

Technology for enabling high-quality, cost-efficient miniaturized cameras devices

- High-yield, reflow-compatible (>30% cost reduction)
- Smaller devices (>50% size reduction)
- Scalable platform: VGA → MPix



**2 High-Volume
Manufacture Licensees**

Imaging & Optics: Image Processing Innovation

Design-In
Technology

Embedded Image
Enhancement

FotoNation® Technology

Technology for enabling
professional quality images
at the push of a button

- Red- & golden-eye correction (>90% detection rate)
- Multiple face detection & tracking (<0.1 seconds lock time)
- Smile & blink detection
- Wrinkle smoothing & blemish correction



2 of Every 3 DSCs
Use Tessera IP



Cell Phones



DSC's



Notebook PCs

Optical Image
Enhancement

OptiML™ Technology

Technology for enabling
high-quality images
without moving parts

- Extended depth of field (EDOF) (3-14MP; in focus from 20cm → ∞)
- Superior low light performance (Up to 250% improvement)
- 3x continuous optical zoom (low F/# at all values, with no moving parts)



3 "Tier 1"
Licensees

Imaging & Optics: Optical Innovation

Products



MEMS

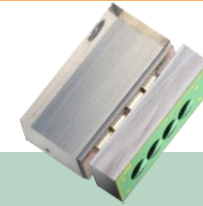
Silicon MEMS

High-performance optical components enabling autofocus in miniaturized camera modules

- High optical performance with small form factor
- Fast, repeatable, accurate movement within 1 micron
- Very low power
- Reduces camera module 'BOM' and simplifies assembly



Used by Industry-Leading Camera Module Manufacturer



Micro-Optics

DigitalOptics™ Lenses

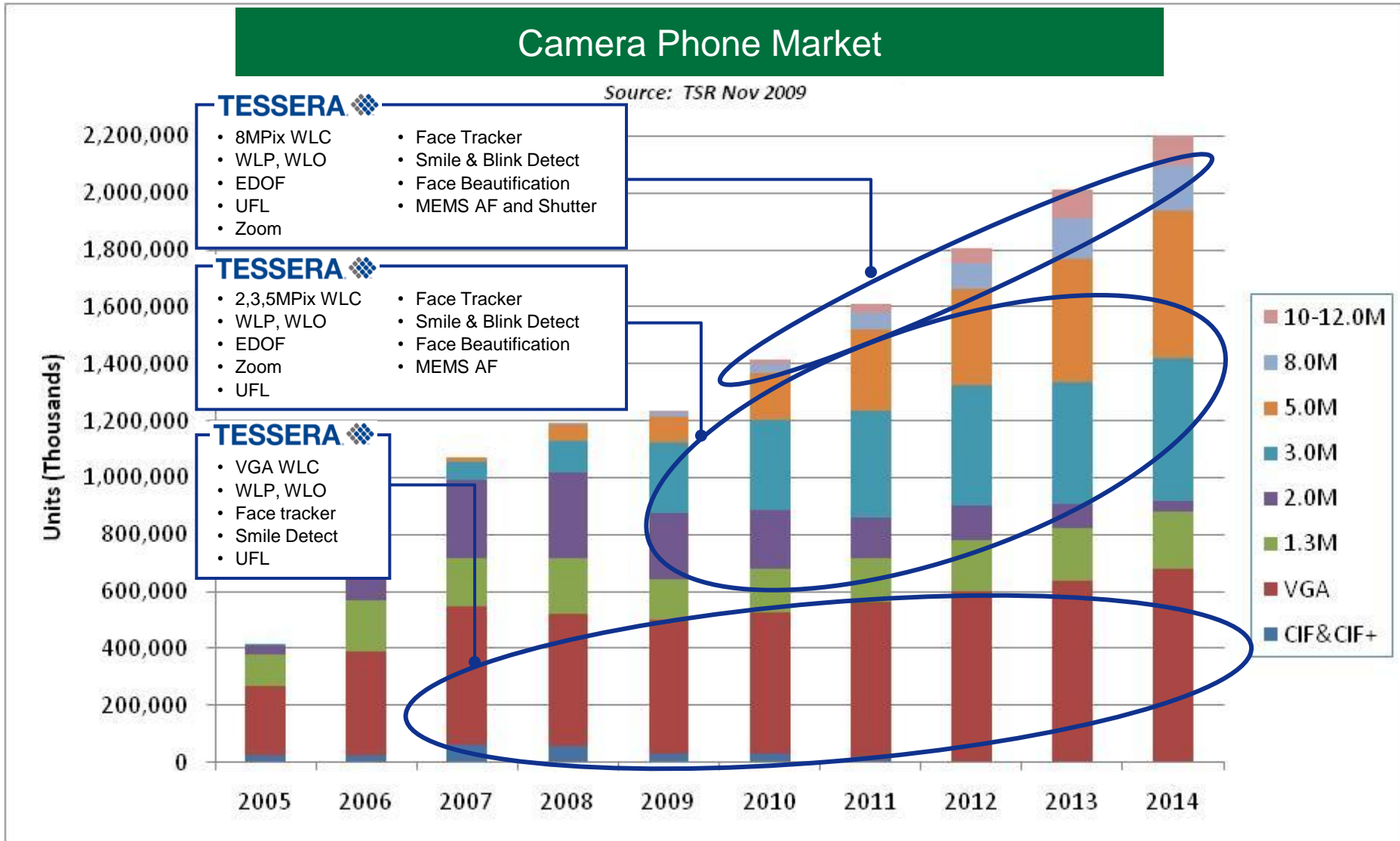
Customized micro-optics enabling greater efficiency, performance and cost savings

- High-efficiency diffractive optical elements
- High-performance refractive optical elements
- Integrated micro-optical sub-assemblies

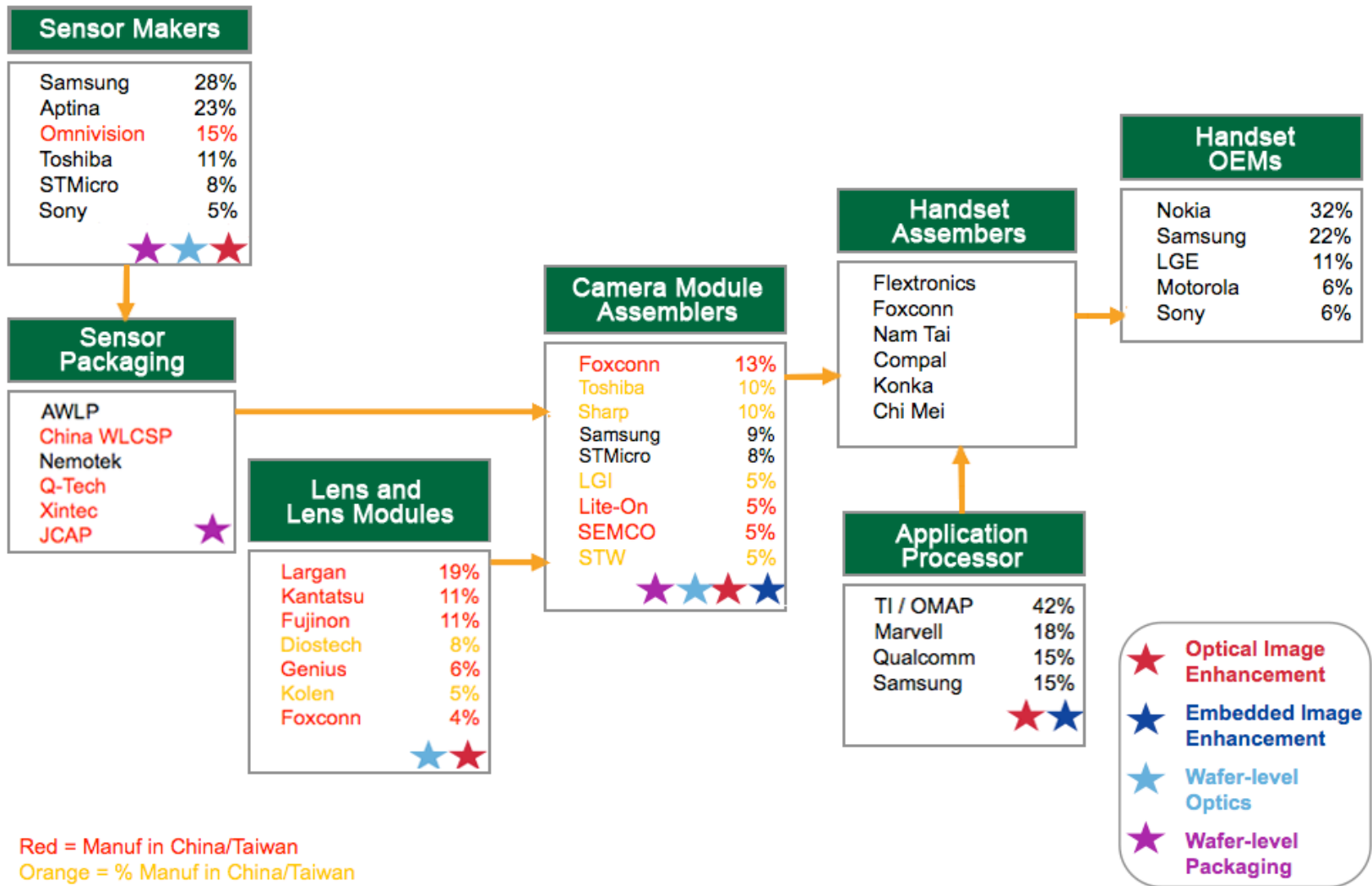


#1 in Litho & Barcode Scanner Lenses

Revenue Sources from Camera Phones



Serving Diverse Needs Across the Supply Chain



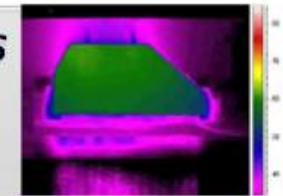
Sources: TSR 2009, Yole 2010

Our Keys to Growth

Extend current license agreements for and market penetration of current CSP and Multi-Chip Package(MCP) technologies.



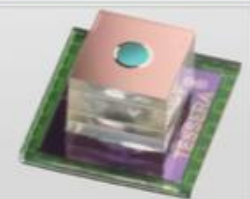
Pursue new business opportunities through licensing and products in next-generation CSP and MCP, Imaging & Optics, and thermal management technologies.



Lead the deployment of intelligent optical engines into Smart Module applications.



Establish Tessera as the de facto Smart Module system architecture.



Broaden our reach as an innovation leader through internal R&D and acquisitions.



Financial Results & Guidance

	Q110 Actual	Q109 Actual *	FY 2009	FY2008	Q210 Guidance
(\$ million, except for per share data)					
Revenue	64.3	114.6	299.4	248.3	67 - 70
Royalties & License Fees	58.9	111.9	286.2	220.3	61.5 – 64.0
Non-GAAP { Cost of Revenue**	3.3	2.3	9.5	13.4	
R&D**	12.5	13.2	52.2	44.2	
SG&A**	14.1	13.5	53.9	52.6	
Operating Expenses excluding Litigation**	29.9	29.0	115.6	110.2	33.8 – 34.9
Litigation	6.6	8.6	26.1	84.3	
Total Operating Expense**	36.5	37.6	141.7	194.5	
Non-GAAP Net Income***	17.8	48.0	101.5	36.2	
Non-GAAP EPS	0.35	0.98	2.02	0.74	
Free Cash Flow per Share****	0.53	1.66		1.10	
Amortization of intangibles	3.5	2.9	12.1	11.1	3.6
Stock-based Compensation	6.9	6.3	27.9	24.1	6.9
Acquired In-Process R&D	-	-	-	2.5	
GAAP Tax	45%	44%	43%	76%	
GAAP Net Income	9.8	39.5	69.8	4.6	
GAAP EPS - Diluted	0.20	0.82	1.42	0.10	

* Q109 included a \$64.1 million payment from Amkor, Inc. for past royalties, of which \$60.6 million was recorded in revenue.

** Excludes Stock based Compensation, Amortization of Acquired Intangibles and Acquired In-process R&D. SG&A excludes Litigation.

*** Excludes Stock based Compensation, Amortization of Acquired Intangibles, Acquired In-process R&D and related tax effects.

**** Free Cash Flow per Share is defined as Operating Cash Flow less Capital Expenditures.

Q210 guidance given on 4/28/10, with subsequent OPEX guidance given on 5/4 for the company's acquisition of Siimpel.

